ISL70003ASEHEV1Z Evaluation Board User Guide

ISL70003ASEHEV1Z

The ISL70003ASEHEV1Z evaluation board is designed to evaluate the performance of the ISL70003ASEH, a TID and SEE hardened 9A synchronous buck regulator IC with integrated MOSFETs intended for space applications. For more detailed information, please refer to the datasheet ISL70003ASEH.

The ISL70003ASEHEV1Z evaluation board accepts a nominal input voltage of 12V and provides a regulated output voltage of 3.3V with output current ranging from 0A to 9A. The output can be quickly adjusted to an alternate voltage using the onboard potentiometer. A PGOOD (Power-Good) signal goes high and lights a green LED to indicate that the output voltage is within a ±11% typical regulation window. A toggle switch (SW1) is provided to conveniently enable or disable the output voltage.

The ISL70003ASEHEV1Z evaluation board can be set to run from the nominal 500kHz or 300kHz internal oscillator of the ISL70003ASEH or synchronized to an external clock. The evaluation board also features a load transient generator to evaluate the dynamic performance of the ISL70003ASEH.

Specifications

- Nominal 3.3V_{IN} - 12V_{IN} operating voltage range
- 9A output current maximum

Key Features

- Adjustable output voltage
- Selectable switching frequency
- Selectable number of output power blocks

What's Inside

The evaluation board contains the following materials:

- ISL70003ASEHEV1Z rev. B evaluation board
- ISL70003ASEH datasheet.
- ISL70003ASEHEV1Z Evaluation Board User Guide AN1897

Recommended Test Equipment

- 0V to 15V power supply with at least 5A current capability
- Electronic load capable of sinking current up to 10A
- Digital Multimeters (DMMs)
- A 500MHz dual or quad trace oscilloscope
- Signal generator (only if evaluating the SYNC function)
- Frequency response analyzer (0.01Hz to 10MHz)

Quick Start

1. Toggle S1 to the OFF position.
2. Turn-on the power supply. Set the output voltage to 12V and set the output current limit to 5A. Turn-off the power supply.
3. Connect the positive lead of the power supply to BAN1 (VIN) and the negative lead of the power supply to BAN4 (GND).
4. Ensure jumpers J6, J7 and J11 are installed. Jumpers should also be connected between pins 2 and 3 of the connectors labeled FSEL, SEL1, SEL2 and DE.
5. Configure one DMM to monitor the input voltage from TP20 to TP17 and another DMM to monitor the output voltage from TP18 to TP19.
6. Connect Channel 1 of the oscilloscope to J1 to monitor the rectangular waveform on the LXx pins.
7. Connect Channel 2 of the oscilloscope to J2 to monitor the output voltage. Ripple voltage is customarily measured with 20MHz bandwidth limiting and AC coupling.
8. Turn-on power supply and toggle S1 to the ON position.
9. Verify the output voltage is 3.3V ±3% and the frequency of the LXx waveform is 500kHz ±10%

Ordering Information

PART NUMBER	DESCRIPTION
ISL70003ASEHEV1Z	ISL70003ASEH radiation and SEE hardened 3V to 12V, 9A synchronous buck regulator evaluation board

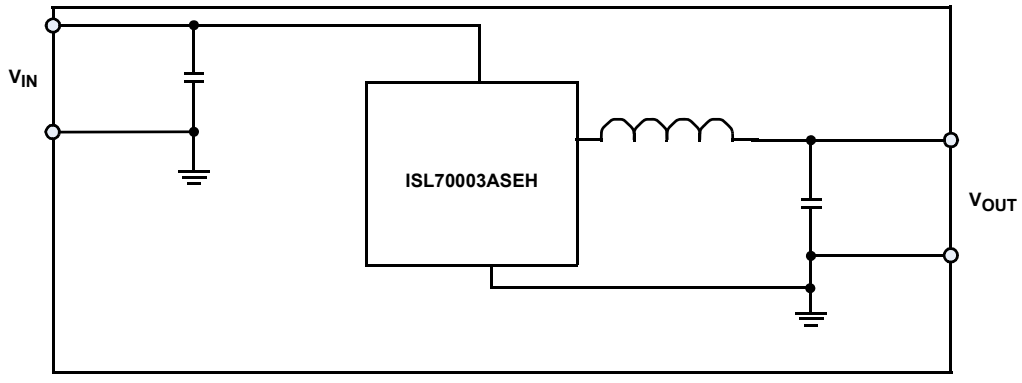


FIGURE 1. ISL70003ASEHEV2Z BLOCK DIAGRAM

FIGURE 2. PHOTOGRAPH OF ISL70003ASEHEV1Z

Evaluating ISL70003ASEH

Load Transient Testing

The board features a high slew rate transient load generator to evaluate the dynamic response of the ISL70003ASEH, as shown in Figure 3. Modern loads such as FPGAs, agitate POL regulators with load transients at slew rates of 10A/µs or higher. The transient generator on the evaluation board is configured to exercise the nominal 3.3V output with a 3A load step at a rising and falling slew rate of 10A/µs.

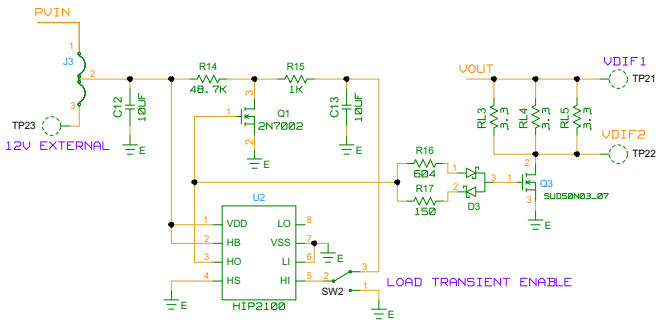


FIGURE 3. LOAD TRANSIENT CIRCUIT

To set up the load generator, perform the following:

1. Ensure SW2 is in the OFF position and short pins 1 and 2 on J3.
2. Follow instructions 1 through 9 in the Quick Start section.
3. The coupling on Channel 2 should be changed to AC coupling and the volts/div setting modified to 50mV/div.
4. The load step may be monitored through the use of a differential probe across test points VDIF1 and VDIF2. If unable to use a differential probe, a regular probe may be placed across VDIFF2 and GND, use the invert function of the oscilloscope to generate the proper polarity.
5. Once a 3.3V output voltage is verified, flip SW2 to the ON position. The load transient generator is now actively exercising the output.

The MOSFET driver, HIP2100, used on the load transient circuit needs 12V on its VDD pin. If evaluating the ISL70003ASEH at a lower input voltage, short pins 2 and 3 on J3 and apply an external 12V supply to TP23, labeled '12V External'. The load step size may be changed through resistors R_{L3} - R_{L5}. The nominal configuration has three 3.3Ω power resistors in parallel. The rising and falling slew rate of the load step is controlled by the gate resistor (R_{12}, R_{13}) and the gate capacitance of Q3. Increasing the resistance decreases the slew rate while decreasing the resistance increases the slew rate. For more detailed information on the load transient generator, please refer to AN1716, "Using the Transient Load Generator on the ISL8200M 2-Phase Power Module Evaluation Board".

Evaluating Other Output Voltages

With a jumper installed on the J7, the ISL70003ASEHEV1Z output voltage is preset to 3.3V. For quick evaluation of other output voltages, the ISL70003ASEHEV1Z provides an on board potentiometer (R_5) on the feedback network, as shown in Figure 4.

To modify the output voltage through R_5, flip SW1 to the OFF position. Open J7 and short J8. Enable the ISL70003ASEH and measure the output voltage with a DMM. Use a small flathead screwdriver to turn the potentiometer until the desired output voltage is achieved.

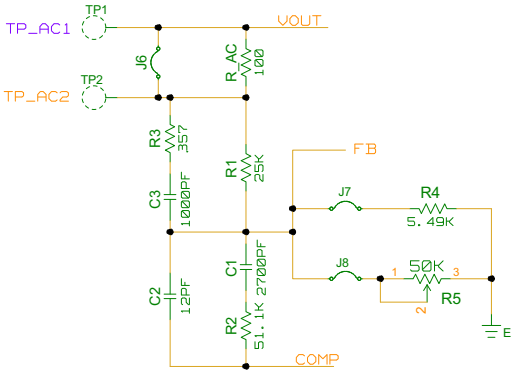


FIGURE 4. FEEDBACK NETWORK CIRCUIT

NOTE: For reliable operation across the entire load and temperature range, it is highly recommended to follow the output filter and loop compensation network design guidelines as listed in the ISL70003ASEH datasheet, once the output voltage has been modified.

Loop Gain Measurements

Loop measurement is needed to analyze the robustness of the power converter design. The evaluation board comes equipped with resistor (R_AC) between the output voltage and the compensation network around the error amplifier, essentially breaking the loop, see Figure 4. Use test points TP1 and TP2 to inject the AC signal differentially across R_AC (with J6 removed) and measure the loop response with the Frequency Response Analyzer. For more detailed information on loop measurement techniques refer to references [1] and [2].

Switching Frequency Selection

The ISL70003ASEH can operate at 300kHz or 500kHz nominal switching frequency. Connector J4 labeled 'FSEL' is used to set the switching frequency. Use Table 1 to configure the evaluation board to the desired switching frequency.

TABLE 1. SETTINGS FOR CONNECTOR FSEL

PINS	CONDITION	SWITCHING FREQUENCY (kHz)
1, 2	SHORT	300
2, 3	SHORT	500

Diode Emulation Mode (DEM)

DEM increases light-load efficiency by turning off the lower MOSFET, thus preventing inductor current from reversing direction and producing unnecessary power loss. Connector J10 labeled 'DE' may be used to place the ISL70003ASEH in DEM. If pins 1 and 2 are shorted on J10 the IC is in DEM, with pins 2 and 3 shorted on J10 the ISL70003ASEH is in continuous conduction mode (CCM).

Active LXx Selections

The ISL70003ASEH can operate with 2, 4 or 10 active LXx blocks active depending on the setting on pins SEL1 and SEL2. This allows the designer to reduce switching losses in low current applications, where all power blocks are not needed to supply the load current. Table 2 compares the state of connectors SEL1, SEL2 with number of active LX pins and the load capability.

TABLE 2. SETTINGS FOR CONNECTORS SEL1 AND SEL2

SEL2 PINS	SEL1 PINS	CONDITION	ACTIVE LXx PINS	LOAD CAPABILITY (T_J = +125°C)
2, 3	2, 3	SHORT	All	9A
2, 3	2, 3	SHORT	5, 6, 7, 8	3.6A
1, 2	1, 2	SHORT	5, 6	1.8A
1, 2	1, 2	SHORT	None	N/A

Changing the Turn-on Voltage

The board features a potentiometer, R_6, in line with resistor PORR2 to modify the on and off threshold voltages of the POR circuit if evaluating the IC at lower input voltages (Figure 5). With the wiper at the top position, essentially shorting R_6, the turn-on threshold is 10.2V and the turn-off threshold is 9V. If the wiper is moved to the lowest position, the turn-on voltage is 2.8V and turn-off voltage is 2.6V. This allows the user to accurately select the turn-on and turn-off voltage for input voltages from 3.3V to 12V.

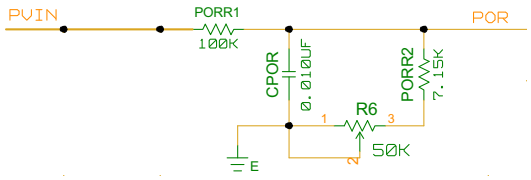


FIGURE 5. POR RESISTOR DIVIDER CIRCUIT

Schematic and BOM

A schematic and BOM of the ISL70003ASEHEV1Z evaluation board are shown in Figure 12 and Table 3, respectively. The schematic indicates the test points, which allow many nodes of the evaluation circuit to be monitored directly. The BOM shows components that are representative of the types needed for a design, but these components are not space-qualified. Equivalent space-qualified components would be required for flight applications.

Layout Guidelines

Layout is very important in high frequency switching converter design. The resulting current transitions from one power device to another and cause voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, radiate noise into the circuit and lead to device overvoltage stress. Careful component layout and printed circuit board design minimizes these voltage spikes. Additionally, careful layout design reduces the impact of load current on the load regulation performance of the output voltage. The following guidelines can be used:

1. Use an eight layer PCB with 2 ounce (70µm) copper or equivalent in thinner layers.
2. 2 layers should be dedicated for ground plane.
3. Top and bottom layers should be used primarily for signals, but can also be used to increase the VIN, VOUT and ground planes as required.
4. Connect all AGND, DGND and PGNDx pins directly to the ground plane. Connect all PVINx pins directly to the VIN portion of the power plane.
5. Locate ceramic bypass capacitors as close as possible to U1. Prioritize the placement of the bypass capacitors on the pins of U1 in the order shown: PVINx, REF, AVDD, DVDD, SS, EN, PGOOD.

6. Locate the output voltage resistive divider and the compensation as close as possible to the FB and VERR pins of the IC. The top leg of the divider should connect directly to the load and the bottom leg of the resistive divider should connect directly to AGND. The junction of the resistive divider should connect directly to the FB pin.
7. Use a small island of copper to connect the LXx pins of U1 to the inductor, L1, to minimize the routing capacitance that degrades efficiency. Separate the island from ground and power planes as much as possible.
8. Keep all signal traces as short as possible.
9. A small series snubber (R_{10} and C_{10}) connected from the LXx pins to the PGNDx pins may be used to dampen ringing on the LXx pins if desired.
10. Optimize load regulation by reducing noise from the power and digital grounds into the analog ground by splitting ground into 3 planes; analog, digital and power. Bypass or ground pins accordingly to their design preferred ground plane. Independently tie each of the analog and digital grounds to power ground via a single trace in a low noise area of the layout. It is recommended that VREFD, VREFOUTS, FSEL, SEL1, SEL2, DE, SS, RTCT be referenced to DGND, that BUFIN, IMON, VREFA, FB, VERR, NI, REF, OCx, be referenced to AGND. To optimize the load regulation performance a Kelvin trace from the inductor output (VOUT) back to the feedback resistor divider and another Kelvin trace from an output capacitor close to the inductor to the IC AGND (PIN7) as shown in Figure 21 will provide a quiet ground reference for the ICs analog circuitry.

Thermal Management for Ceramic Package

For optimum thermal performance, place a pattern of vias on the top layer of the PCB directly underneath the IC. Connect the vias to the plane which serves as a heatsink. To ensure good thermal contact, thermal interface material such as a Sil-Pad or thermally conductive epoxy should be used to fill the gap between the vias and the bottom of the IC of the ceramic package.

Lead Strain Relief

The package leads protrude from the bottom of the package and the leads need forming to provide strain relief. On the ceramic bottom package R64.A, the Sil-pad or epoxy may be used to fill the gap left between the PCB board and the bottom of the package when lead forming is completed. On the heatsink option of the package R64.C, the lead forming should be made so that the bottom of the heatsink and the formed leads are flush.

Heatsink Mounting Guidelines

The R64.C package option has a heatsink mounted on the underside of the package. The following JESD-51x series guidelines may be used to mount the package:

1. Place a thermal land on the PCB under the heatsink.
2. The land should be approximately the same size as to 1mm larger than the 10.16x10.16mm heatsink.
3. Place an array of thermal vias below the thermal land.
   - Via array size: ~9x9 = 81 thermal vias.
   - Via diameter: ~0.3mm drill diameter with plated copper on the inside of each via.
   - Via pitch: ~1.2mm.
   - Vias should drop to and contact as much metal area as feasible to provide the best thermal path.

Heatsink Mounting Materials

In the case of electrically conductive mounting methods (conductive epoxy, solder, etc.) the thermal land, vias and connected plane(s) below must be the same potential as pin 50. This board uses solder to connect the heatsink to the thermal land pattern underneath the IC. The vias on the thermal land connect to the underlying grounds for thermal relief.

In the case of electrically nonconductive mounting methods (nonconductive epoxy), the heatsink and pin 50 could have different electrical potential than the thermal land, vias and connected plane(s) below.

References

[1] Venable Industries, Venable Technical Paper #1, “Testing Power Sources for Stability” http://venable.biz/uploads/files/01-Technical-Paper-Testing-Power-Sources-for-Stability.pdf

[2] Dr. Ray Ridley, “Loop Gain Measurement Injection Technique” http://www.ridleyengineering.com/ap300-loop-injection.html

Typical Performance Curves

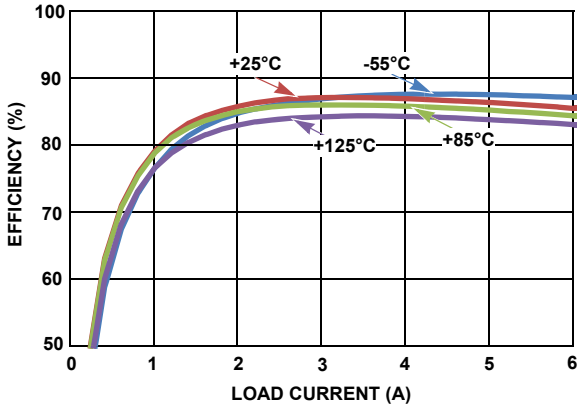


FIGURE 6. EFFICIENCY vs LOAD vs TEMPERATURE
V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 500kHz

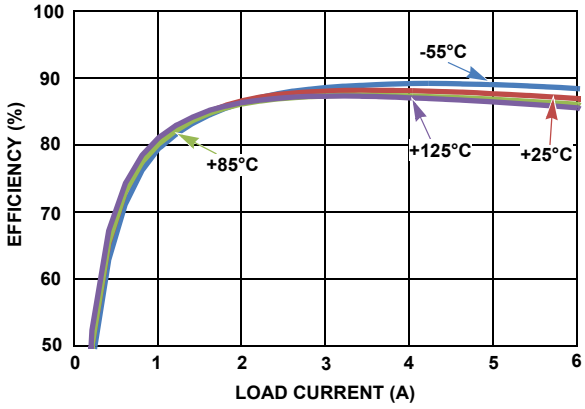


FIGURE 7. EFFICIENCY vs LOAD vs TEMPERATURE
V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 300kHz

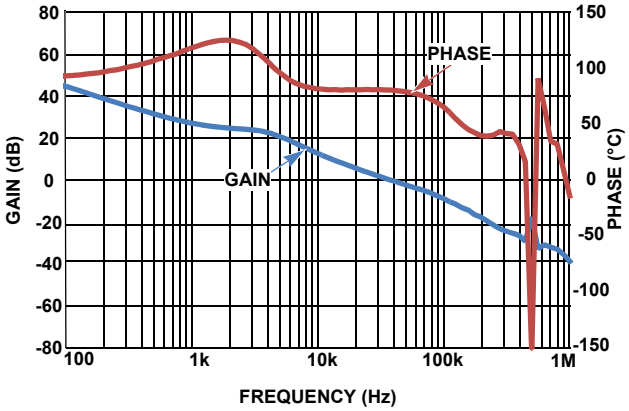


FIGURE 8. GAIN AND PHASE PLOTS, 0A LOAD, CCM
V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 500kHz

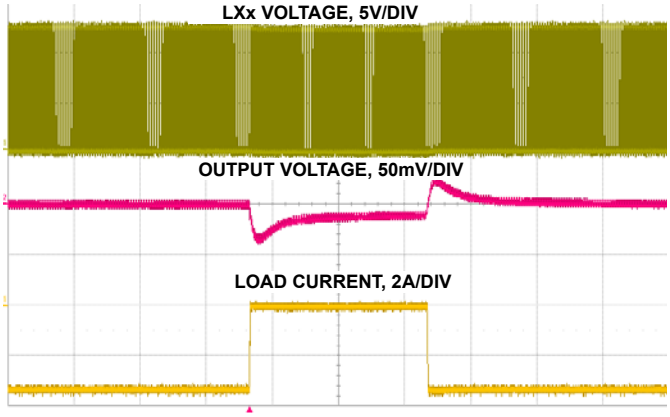


FIGURE 9. 3A LOAD TRANSIENT RESPONSE
V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 500kHz

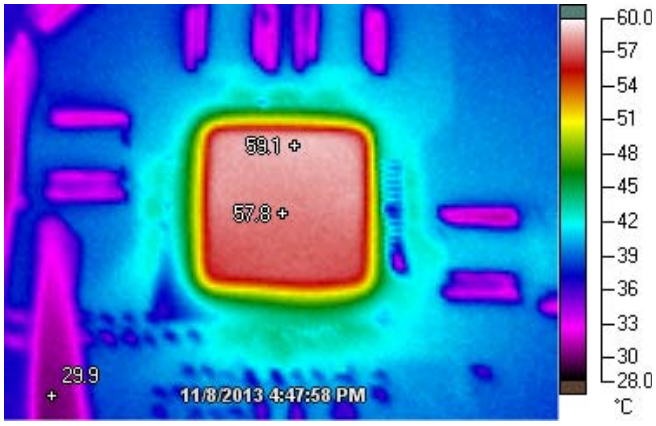


FIGURE 10. THERMAL IMAGE OF REGULATOR, 6A LOAD
V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 500kHz, T_A = +25°C

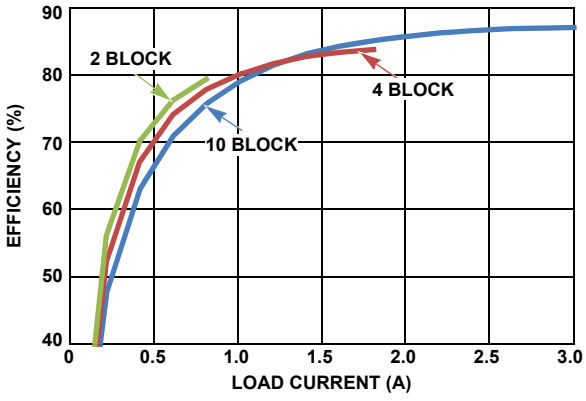


FIGURE 11. EFFICIENCY vs LOAD vs # ACTIVE LX_X BLOCKS
V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 500kHz

ISL70003ASEHEV1Z Schematics

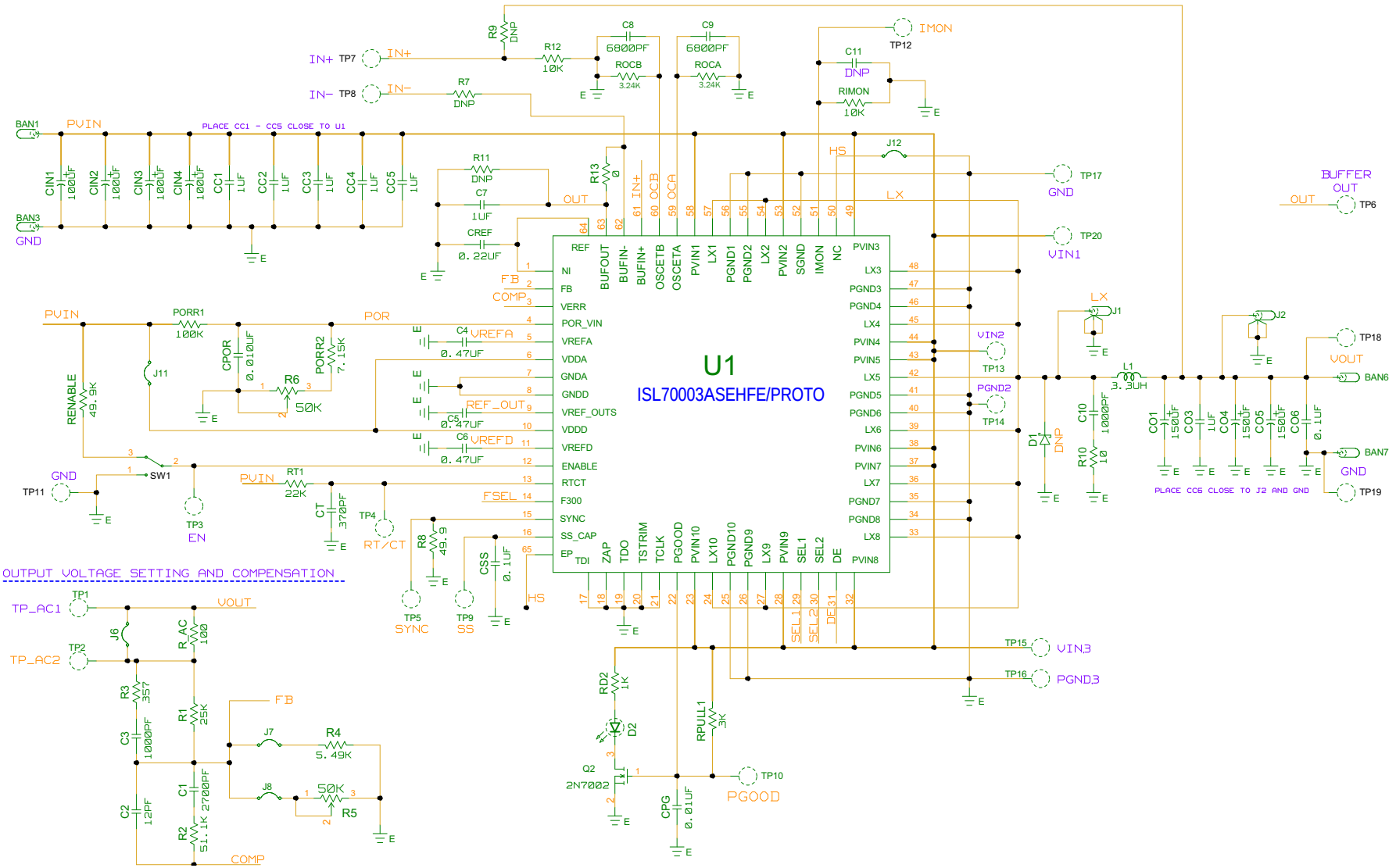
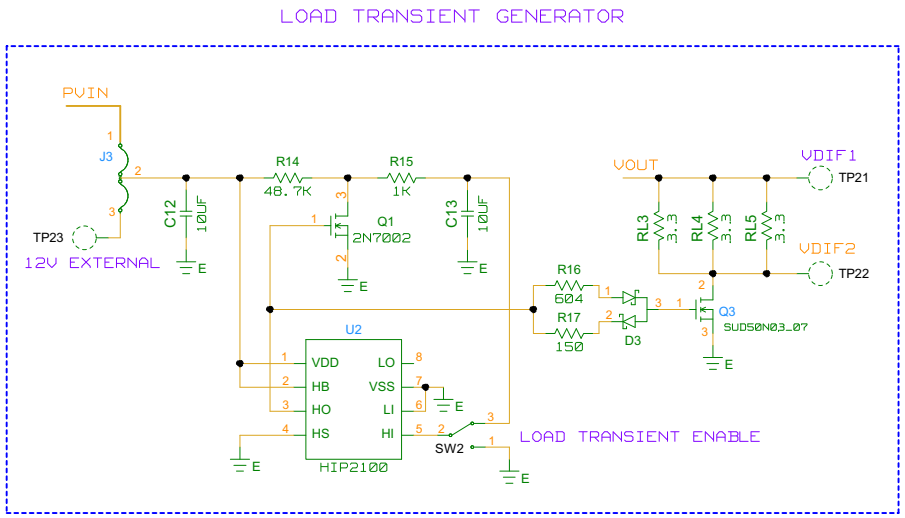


FIGURE 12. ISL70003ASEHFE/PROTO

ISL70003ASEHEV1Z Schematics (Continued)



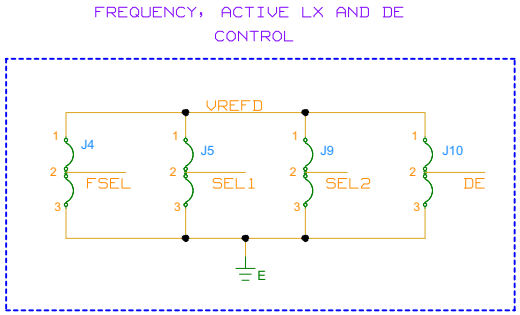


FIGURE 13. ISL70003ASEH LOAD TRANSIENT GENERATOR AND CONTROL

TABLE 3. ISL70003ASEHEV1Z BOM

REFERENCE DESIGNATOR	QTY	DESCRIPTION	PART NUMBER	MANUFACTURER
CT	1	CAP, SMD, 1206, 370pF, 50V, 1%, C0G, ROHS	12065A371FAT2A	AVX
C3, C10	2	CAP, SMD, 0603, 1000pF, 50V, 5%, C0G, ROHS	GRM1885C1H102JA01D	MURATA
CPG	1	CAP, SMD, 0603, 0.01µF, 16V, 10%, X7R, ROHS	C0603X7R160-103KNE	VENKEL
CO6, CSS	2	CAP, SMD, 0603, 0.1µF, 50V, 10%, X7R, ROHS	06035C104KAT2A	AVX
C7	1	CAP, SMD, 0603, 1.0µF, 10V, 10%, X7R, ROHS	0603ZC105KAT2A	AVX
C2	1	CAP, SMD, 0603, 12pF, 50V, 5%, NP0, ROHS	C1608C0G1H120J	TDK
CREF	1	CAP, SMD, 0603, 0.22µF, 16V, 10%, X7R, ROHS	C1608X7R1C224K	TDK
C1	1	CAP, SMD, 0603, 2700pF, 50V, 10%, X7R, ROHS	ECJ-1VB1H272K	PANASONIC
C8, C9	2	CAP, SMD, 0603, 6800pF, 16V, 10%, X7R, ROHS	C0603X7R160-682KNE	VENKEL
C11	0	CAP, SMD, 0603, DNP-PLACE HOLDER, ROHS		
C12, C13	2	CAP, SMD, 0805, 10µF, 16V, 10%, X5R, ROHS	C0805X5R160-106KNE	VENKEL
CC1-CC5, CO3	6	CAP, SMD, 2225, 1µF, 200V, 10%, X7R, ROHS	VJ2225Y105KXCAT	VISHAY/VITRAMON
C4-C6	3	CAP, SMD, 2225, 0.47µF, 100V, 10%, X7R, ROHS	C2225C474K1RACTU	KEMET
CIN1-CIN4	4	CAP, TANT, SMD, 7.3x4.3x4, 100µF, 25V, 10%, 300mΩ, ROHS	T491X107K025AT	KEMET
CO1, CO4, CO5	3	CAP TANT, LOW ESR, SMD, D, 150µF, 10V, 20%, 6mΩ, ROHS	T530D157M010ATE006	KEMET
CPOR	1	CAP, SMD, 1210, 0.01µF, 500V, 10%, X7R, ROHS	VJ1210Y103KXEAT5Z	VISHAY/VITRAMON
L1	1	COIL-PWR INDUCTOR, SMD, 12.9x13.2, 3.3µH, 20%, 12A, ROHS	IHLP5050CEER3R3M01	VISHAY
J1, J2	2	CONN-SCOPE PROBE TEST PT, COMPACT, PCB MNT, ROHS	131-4353-00	TEKTRONIX
TP1-TP23	23	CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS	5002	KEYSTONE
BAN1, BAN3, BAN6, BAN7	4	CONN-JACK, MINI BANANA, 0.175 PLUG, NICKEL/BRASS, ROHS	575-4	KEYSTONE
J3-J5, J9, J10	5	CONN-HEADER, 1x3, BREAKAWY 1x36, 2.54mm, ROHS	68000-236HLF	BERG/FCI
J6, J7, J8, J11, J12	5	CONN-HEADER, 1x2, RETENTIVE, 2.54mm, 0.230x0.120, ROHS	69190-202HLF	BERG/FCI
J6, J7, J8, J11, J12	5	CONN-JUMPER, SHORTING, 2PIN, BLACK, GOLD, ROHS	SPC02SYAN	SULLINS
D3	1	DIODE-SCHOTTKY, SMD, SOT23, 3P, 30V, 200mA, DUAL DIODE	BAT54S	FAIRCHILD
D1	1	DIODE-RECTIFIER, SMD, SMC, 2P, 20V, 3A, ROHS	MBRS320T3G	ON SEMICONDUCTOR
D2	1	LED, SMD, 0603, GREEN CLEAR, 2V, 20mA, 571nm, 35mcd, ROHS	LTST-C190KGKT	LITEON/VISHAY
U2	1	IC-HI FREQ BRIDGE DRIVER, 8P, SOIC, 100V, ROHS	HIP2100IBZ	INTERSIL
U1	1	IC-RAD-HARD12A BUCK REGULATOR, 64P, CQFP, ROHS	ISL70003ASEHFE/PROTO	INTERSIL
Q1, Q2	2	TRANSISTOR, N-CHANNEL, 3LD, SOT-23, 60V, 115mA, ROHS	2N7002-7-F	DIODES, INC.
Q3	1	TRANSISTOR-MOS, N-CHANNEL, SMD, TO-252, 30V, 90A, ROHS	SUD50N03-06AP-E3	VISHAY
R5, R6	2	POT-TRIM, TH, 50k, 1/2W, 10%, 3P, 3/8 SQ., 25TURN, ROHS	3296W-1-503LF	BOURNS
RT1	1	RES, SMD, 0603, 22k, 1/10W, 0.1%, 25ppm, THINFILM, ROHS	ERA-3AEB223V	PANASONIC
ROCA, ROCB	2	RES, SMD, 0603, 3.24k, 1/10W, 0.1%, 25ppm, ROHS	MCT06030D3241BP500	VISHAY
R7, R9, R11	0	RESISTOR, SMD, 0603, 0.1%, MF, DNP-PLACE HOLDER		
R13	1	RES, SMD, 0402, 0Ω, 1/16W, 5%, TF, ROHS	CR0402-16W-00T	VENKEL
R_AC	1	RES, SMD, 0603, 100Ω, 1/10W, 1%, TF, ROHS	CR0603-10W-1000FT	VENKEL
R15, RD2	2	RES, SMD, 0603, 1k, 1/10W, 1%, TF, ROHS	ERJ-3EKF1001V	PANASONIC
R12	1	RES, SMD, 0603, 10k, 1/10W, 1%, TF, ROHS	RK73H1JT1002F	KOA
R17	1	RES, SMD, 0603, 150Ω, 1/10W, 1%, TF, ROHS	CR0603-10W-1500FT	VENKEL
R1	1	RES, SMD, 0603, 24.9k, 1/10W, 1%, TF, ROHS	ERJ-3EKF2492V	PANASONIC

TABLE 3. ISL70003ASEHEV1Z BOM (Continued)

REFERENCE DESIGNATOR	QTY	DESCRIPTION	PART NUMBER	MANUFACTURER
RPULL1	1	RES, SMD, 0603, 3k, 1/10W, 1%, TF, ROHS	RC0603FR-073KL	YAGEO
R3	1	RES, SMD, 0603, 357Ω, 1/10W, 1%, TF, ROHS	ERJ-3EKF3570V	PANASONIC
R14	1	RES, SMD, 0603, 48.7k, 1/10W, 1%, TF, ROHS	ERJ-3EKF4872V	PANASONIC
RENABLE	1	RES, SMD, 0603, 49.9k, 1/10W, 1%, TF, ROHS	CR0603-10W-4992FT	VENKEL
R8	1	RES, SMD, 0603, 49.9Ω, 1/10W, 1%, TF, ROHS	CR0603-10W-49R9FT	VENKEL
R2	1	RES, SMD, 0603, 51.1k, 1/10W, 1%, TF, ROHS	CR0603-10W-5112FT	VENKEL
R4	1	RES, SMD, 0603, 5.49k, 1/10W, 1%, TF, ROHS	CR0603-10W-5491FT	VENKEL
R16	1	RES, SMD, 0603, 604Ω, 1/10W, 1%, TF, ROHS	ERJ-3EKF6040V	PANASONIC
PORR2	1	RES, SMD, 0603, 7.15k, 1/10W, 1%, TF, ROHS	ERJ-3EKF7151V	PANASONIC
RIMON	1	RES, SMD, 0805, 10k, 1/8W, 1%, TF, ROHS	CR0805-8W-1002FT (pb-free)	VENKEL
PORR1	1	RES, SMD, 0805, 100k, 1/8W, 1%, TF, ROHS	CR0805-8W-1003FT	VENKEL
R10	1	RES, SMD, 1206, 10Ω, 1/4W, 1%, TF, ROHS	CR1206-4W-10R0FT	VENKEL
RL3-RL5	3	RES, SMD, 2512, 3.3Ω, 1W, 1%, TF, ROHS	SR73H3AT3R30F	KOA
SW1, SW2	2	SWITCH-TOGGLE, SMD, 6PIN, SPDT, 2POS, ON-ON, ROHS	GT11MSCBE	ITT/C&K

ISL70003ASEHEV1Z Layout

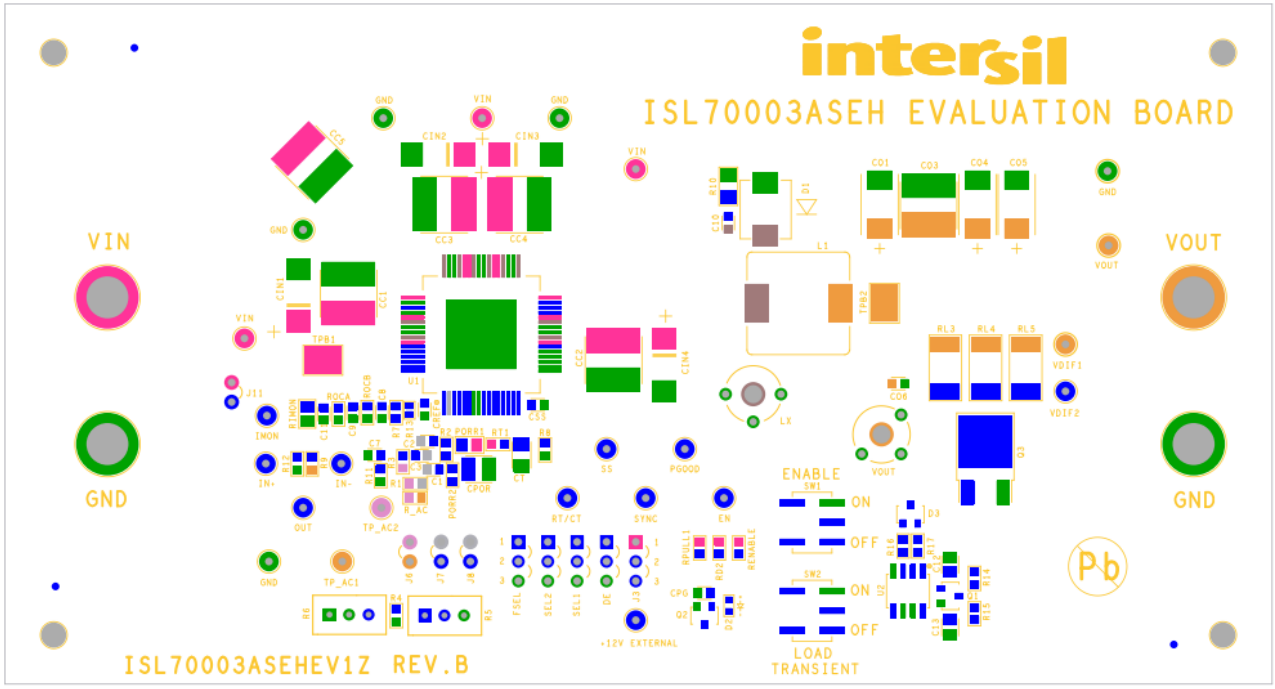


FIGURE 14. TOP SILKSCREEN

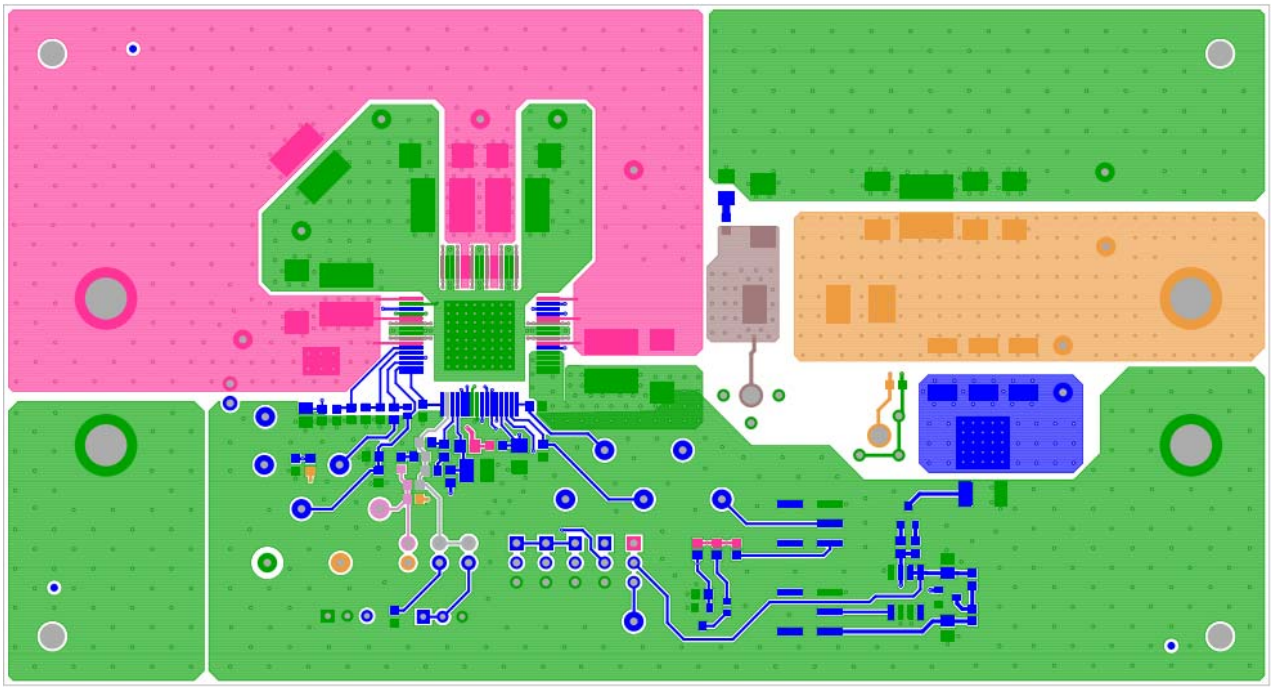


FIGURE 15. TOP LAYER

ISL70003ASEHEV1Z Layout (Continued)

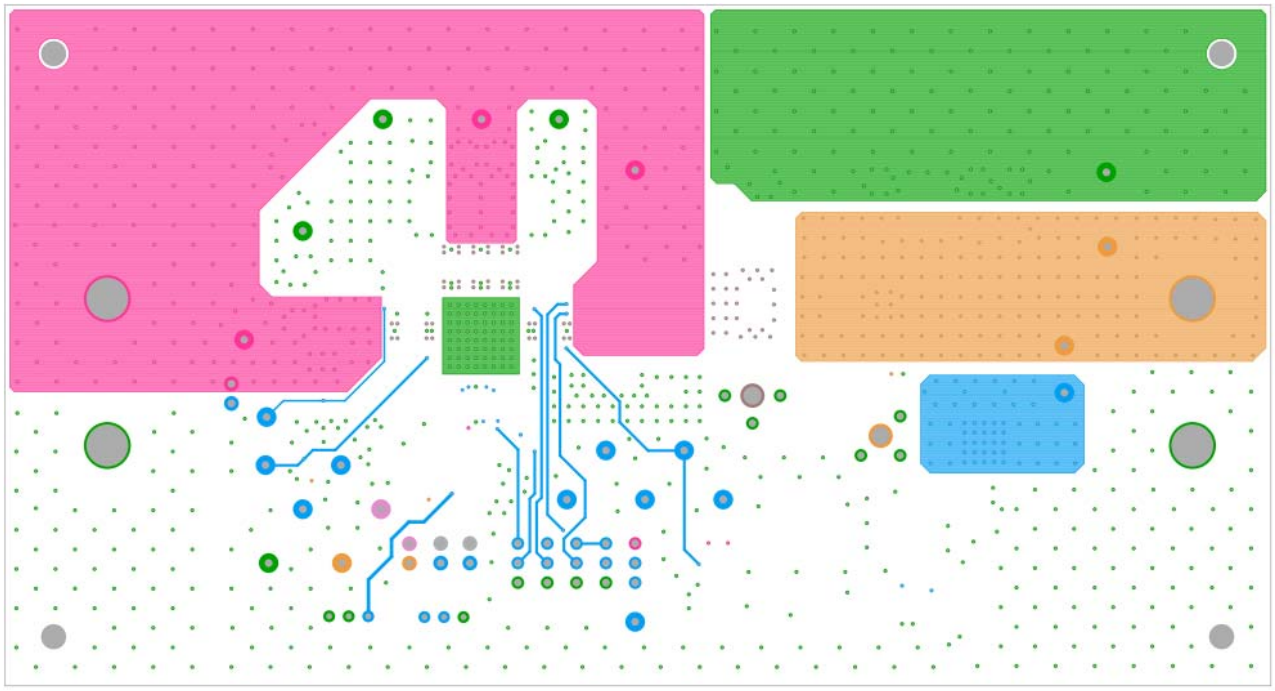


FIGURE 16. LAYER 2

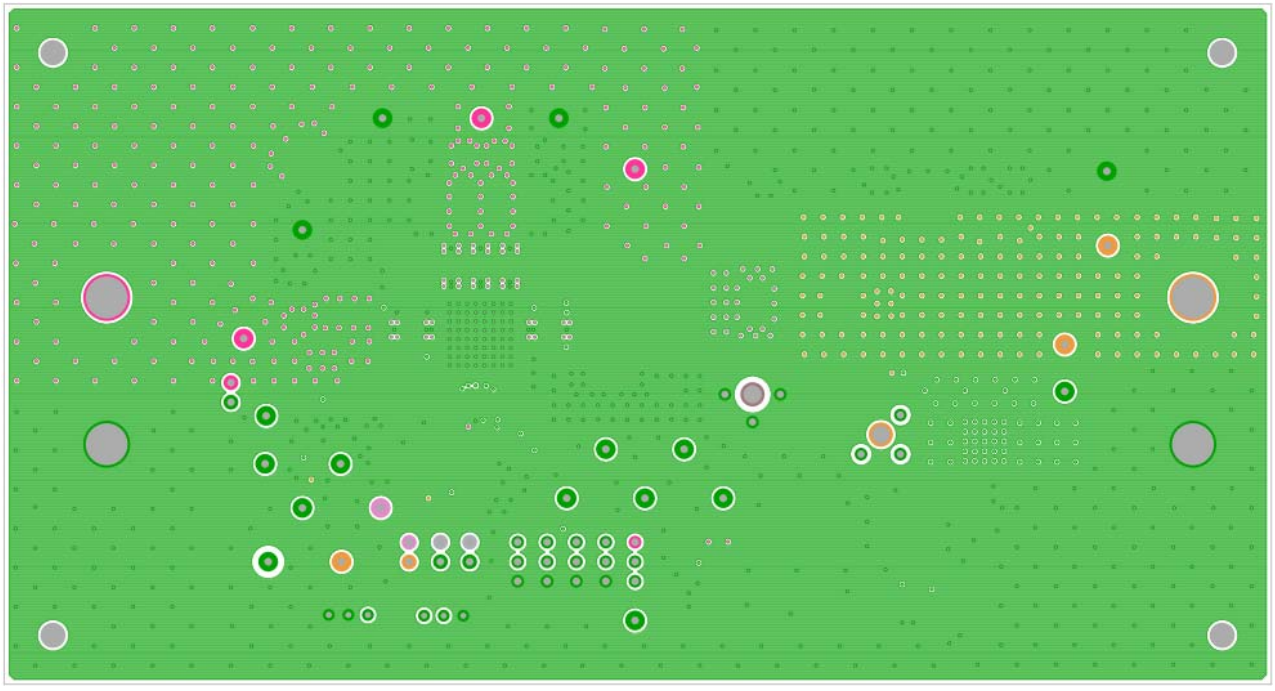


FIGURE 17. LAYER 3

ISL70003ASEHEV1Z Layout (Continued)

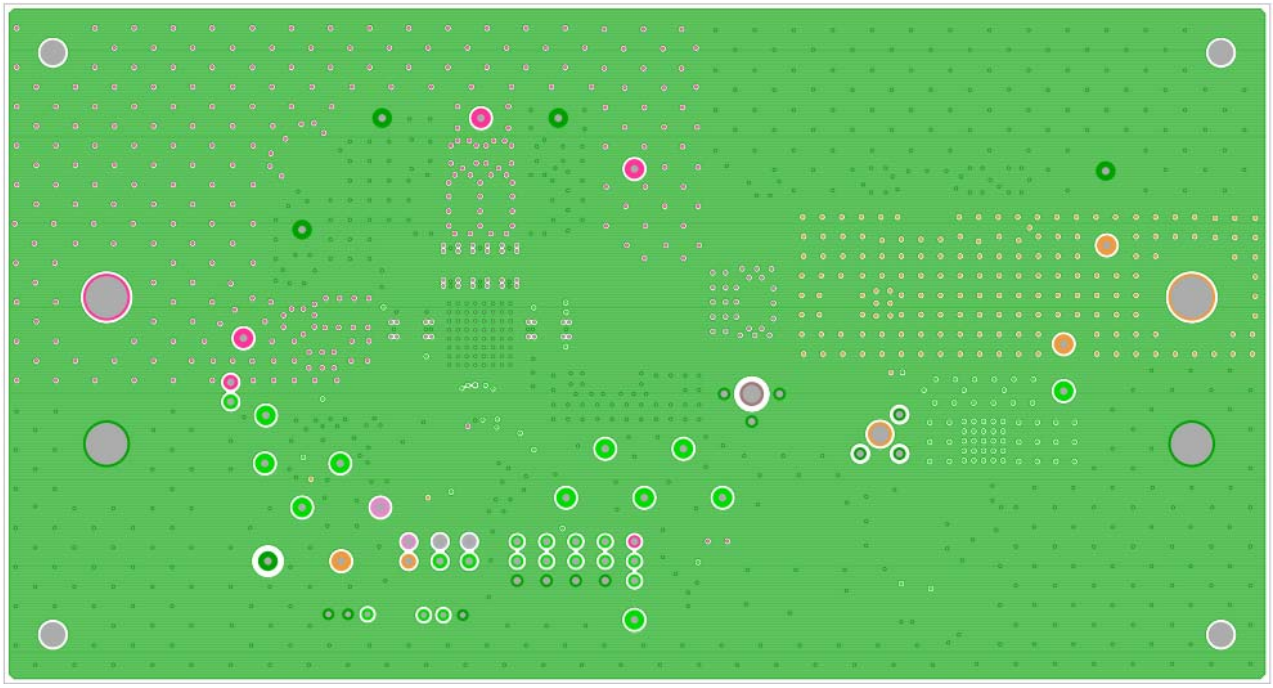


FIGURE 18. LAYER 4

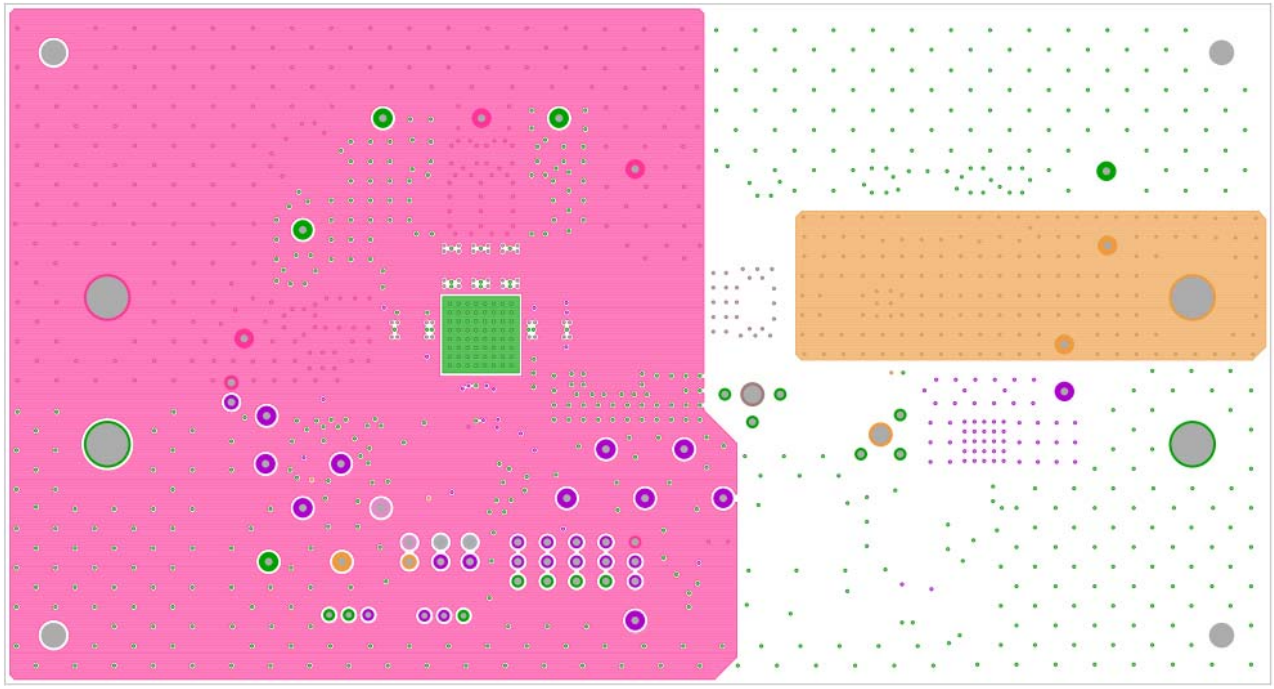


FIGURE 19. LAYER 5

ISL70003ASEHEV1Z Layout (Continued)

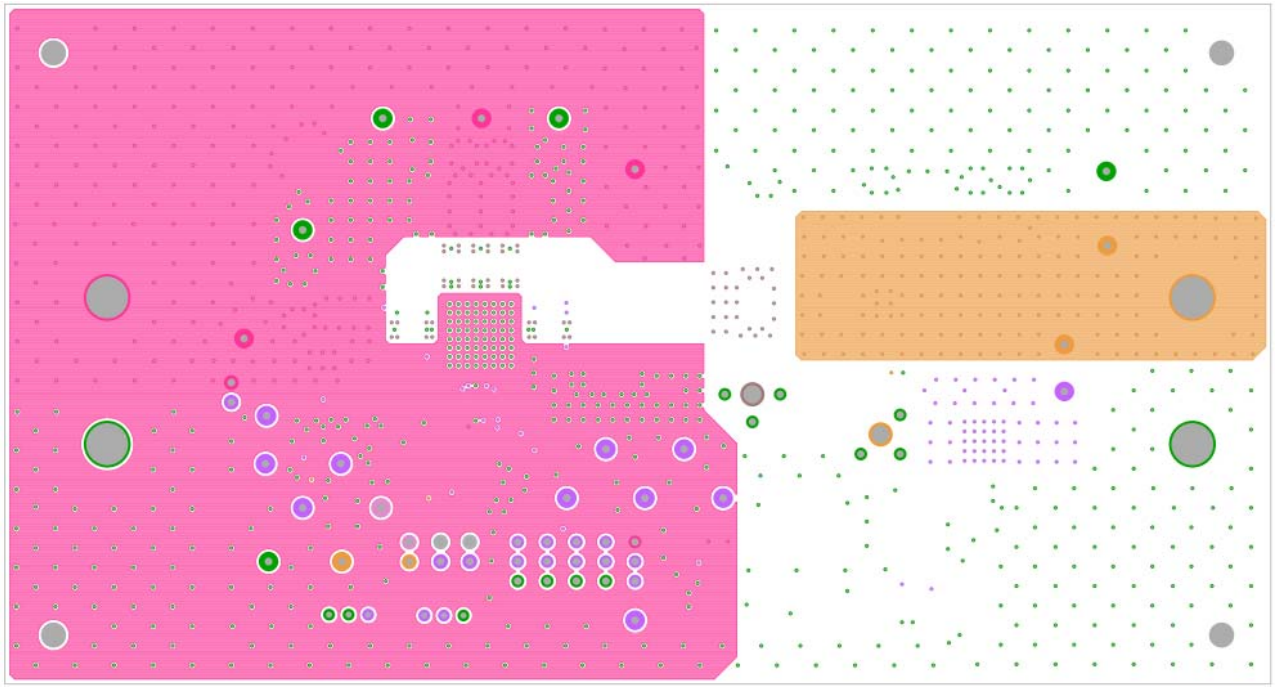


FIGURE 20. LAYER 6

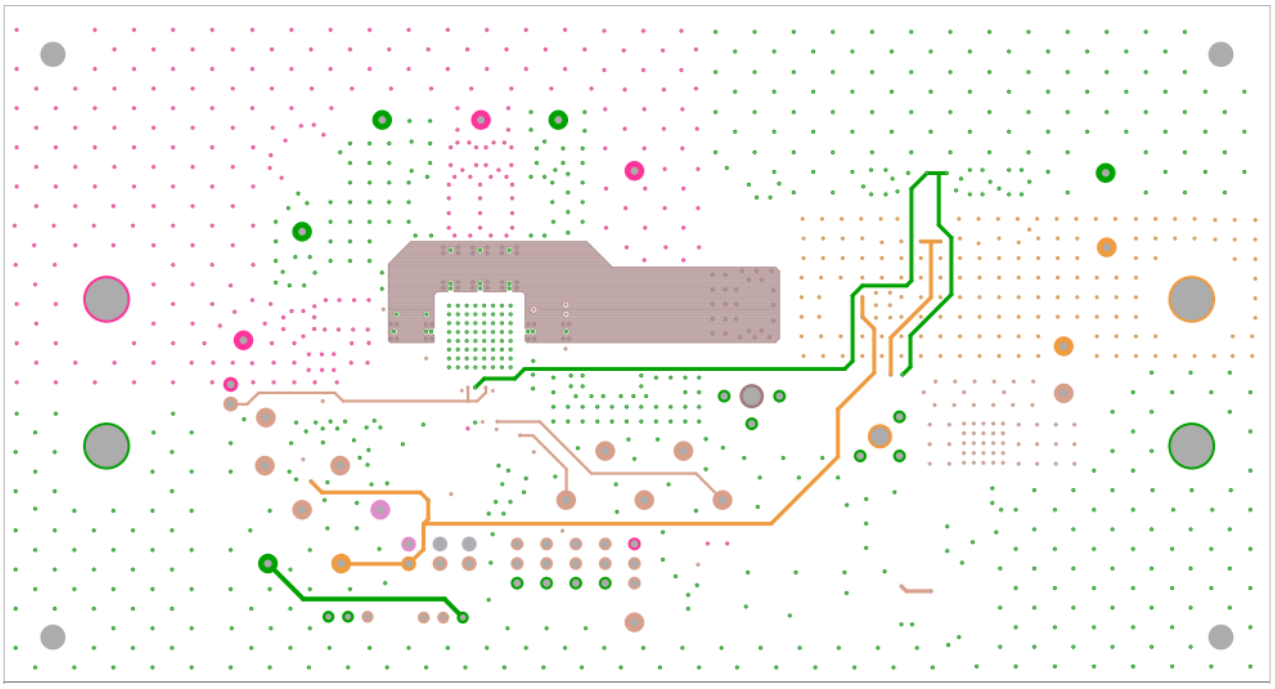


FIGURE 21. LAYER 7

ISL70003ASEHEV1Z Layout (Continued)

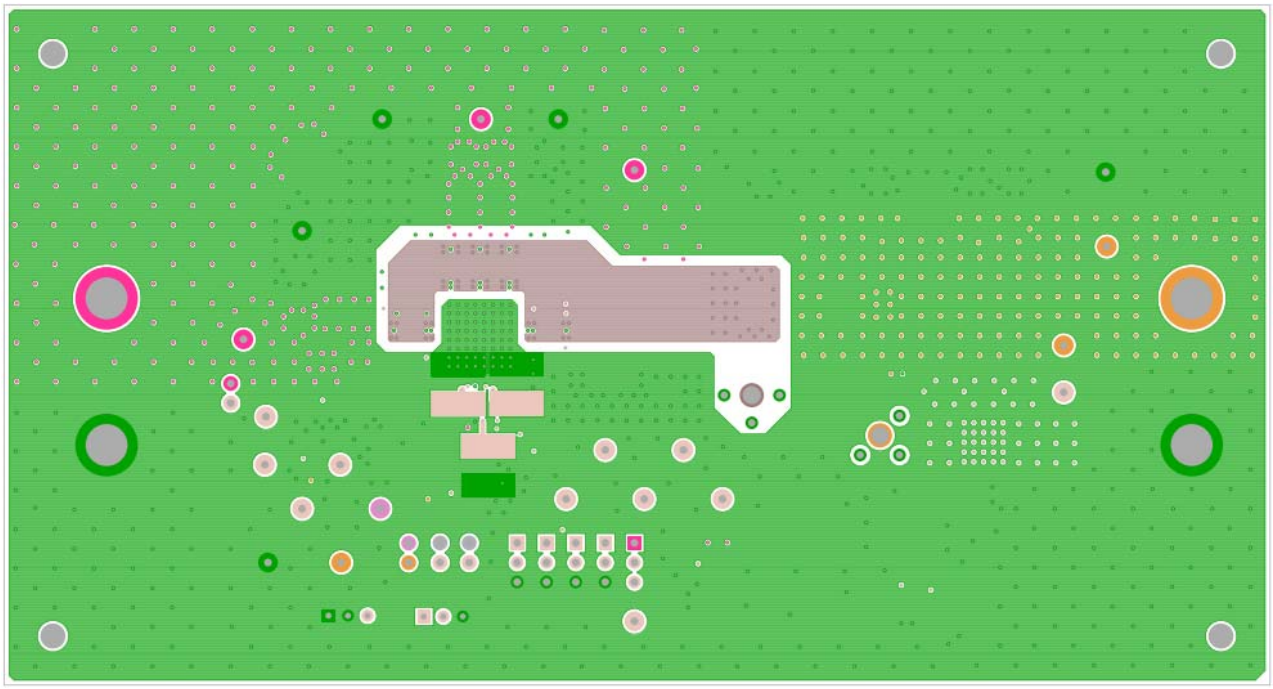


FIGURE 22. LAYER 8

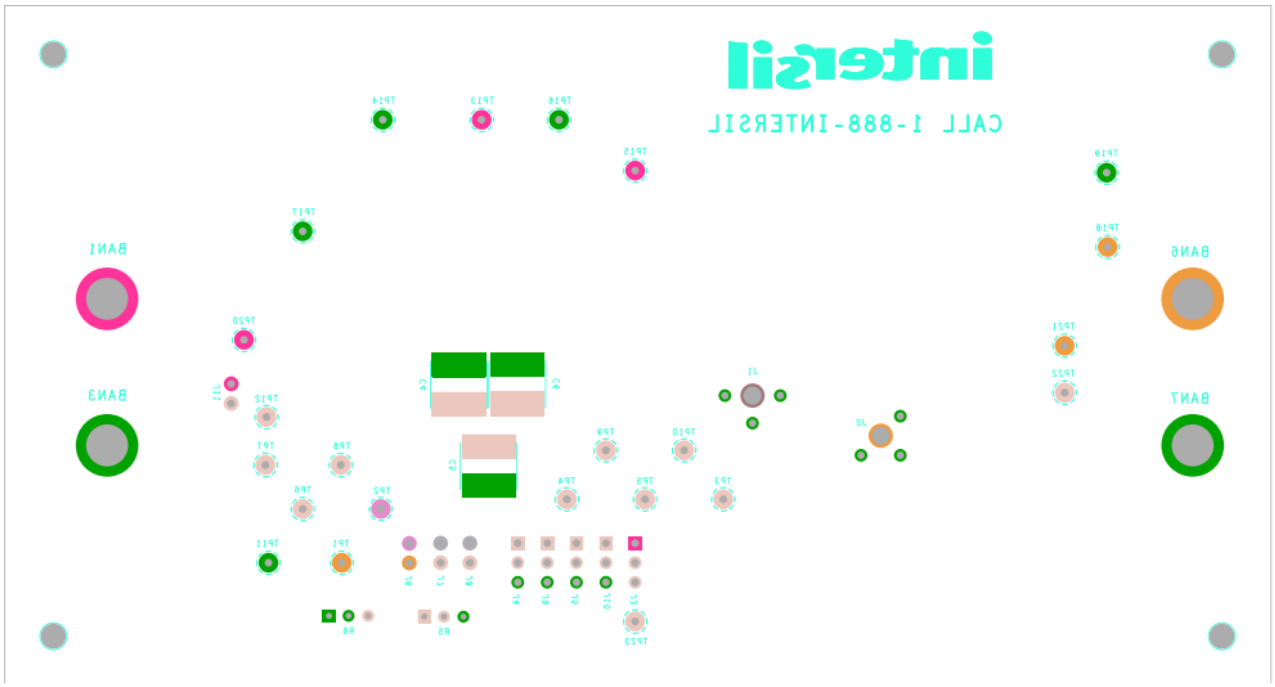


FIGURE 23. BOTTOM SILKSCREEN